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STRATEGIC METHODOLOGIES FOR LOW POWER VLSI DESIGNS AND EFFECTIVENESS OF POWER ESTIMATION TOOL: AN ANALYSIS

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Abstract

Recently power dissipation is becoming an important constraint in design process. In that Low power design is becoming a new era in VLSI technology, as it impacts many applications. With the increase in speed, mobility and miniaturization of electronic devices, the power consumption of these devices has become major design factor. Especially for mobile devices the power consumption determines the battery life time.Therefore the designers, consumers, as well as environmental considerations demand a reduction of power dissipation in digital circuits. Digital circuits consist of a number of interconnected logic gates which together perform a function on one or more input signals. Every time an input signal changes it propagates via the gates causing signal transition in every place where the signals propagate. This causes current to charge or discharge the capacitive load of CMOS gates which results in power dissipation.This article main focus on strategic methodologies for low power VLSI designs and its effectiveness.

1. OVERVIEW

VLSI is a phrase that stands for "Very Large Scale Integration" is the process of creating an integrated circuit by combining millions of transistors in to a single silicon chip. VLSI field involves packing more and more logic devices into smaller and smaller areas because it is one of the basic building blocks of today's higher end devices and advanced technologies. Circuits that would have taken a full board of space can now be placed into a small space of few millimeters which has opened more opportunity to do things that were not possible before. VLSI circuits are used almost everywhere such as automobiles, different computer systems, car, digital camera, cell-phones and many other electronic products. According to Moore's law, integrated circuits capability increases exponentially every year, especially in computation power, area and yield[1-6].

Dealing with VLSI circuits

Digital VLSI circuits are basically CMOS based. Blocks like latches and gates are implemented which is different from what have been seen so far, but the behavior remains same. Miniaturization involves new ideas to be considered. A lot of thought has to go into actual implementation as well as design. Some of the factors involved are as follows:

- **Circuit delays**

Large complicated circuits running at very high frequencies have one big problem to tackle - the problem of delay in propagation of signals through gates and wire even for few micrometers. Also operation speed takes more time as delays add up. Another effect of high frequencies is increased consumption of power. This has two-fold effect - devices consume batteries quickly and an increase in heat dissipation. Taking into consideration that surface areas also have decreased, heat is a major threat to circuit stability.

- **Layout**

Laying out the circuit components is a task common to all branches of electronics. There are many possible ways to do this like, multiple layers of different materials on the same silicon and different arrangements of smaller parts for the same component and so on. The power dissipation and speed in a circuit present a trade-off and optimizing one affects another. The selection between the two is determined by the layout of the circuit components. This will also affect the fabrication of chips.

The VLSI design Process

All modern digital designs start with a designer writing a hardware description of the IC (using HDL or Hardware Description Language) in Verilog/VHDL. Both essentially describes the hardware (logic gates, Flip-Flops, counters etc) interconnect of the circuit blocks and its functionality. CAD tools are also available to synthesize circuits based on HDL. VHDL means "VHSIC Hardware Description Language", where VHSIC stands for "Very High Speed Integrated Circuit".

By using these languages, circuits are designed at higher-level. One describes behavioral description that means what the circuit is expected to do and the other tells about structure and how the circuit is made. Other languages such as Verilog also work in a similar fashion. Both languages are used to generate a very low-level description that actually spells out how all this is

to be fabricated on the silicon chips. Most of the time VLSI designs are classified into three categories.

- **Analog**

Analog IC design involves small transistor precision circuits like as amplifiers, data converters, filters, phase locked loops, sensors etc.

- **Asics or application specific integrated circuits**

Progress in the fabrication of IC has enabled us to create fast and powerful circuits in very smaller devices. This also means that more functionality could be packed into the same area. These are integrated circuits that are created for specific purposes and each device is created to do a particular job. The common application area is DSP signal filters, in Image compression. Consider the fact that the digital wrist watch normally consists of a single IC doing all the time keeping jobs as well as extra features like calendar, Low Power GPS Receiver etc.

- **Soc or System on a chip**

Soc systems are highly complex mixed signal circuits (digital and analog all on single chip) and very much used in embedded systems, wireless chip etc.

Interconnect

Interconnect plays an increasing role in determining the entire area of chip, delay, power dissipation and must be considered early, i.e. during the design process itself. Once the devices are fabricated completely, they must be electrically connected to each other to make circuits and communicate with outside world. The wires are used to connect the devices together are called interconnect which play a major role in the performance of modern system. Figure 1 and 2 shows the schematic diagram and comparison of interconnects structure.

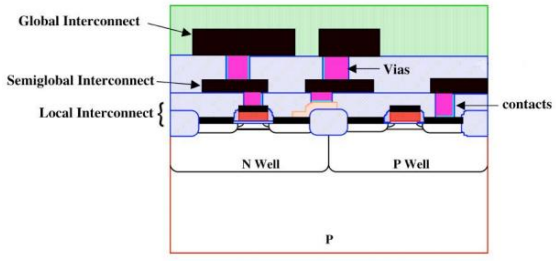

Figure 1: Interconnect Structure

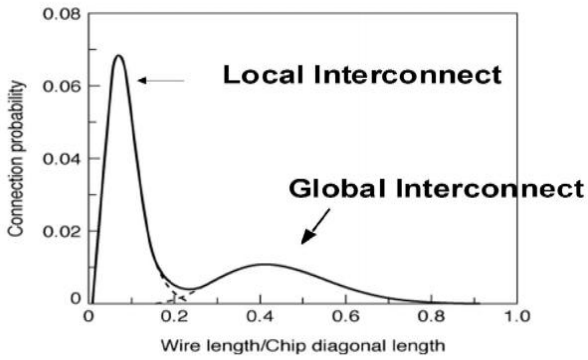

Figure 2: Comparison of interconnect

2. LOW POWER VLSI DESIGN

Latest developments in the field of VLSI Technology show an increasing interest in analog circuit design. The main aim of analog integrated circuits (ICs) is to satisfy circuit specifications through circuit architectures with the required performance. They can be used either as "stand-alone" topologies or connected to the digital part to implement mixed analog-digital functions, utilized in a wide field of applications. Though numerous researchers predicted a reduced utilization of analog architectures and an increased development of the digital counterpart, analog circuitry continues to be a necessary part of the technology.

In fact, analog circuits are needed in many VLSI systems such as filters, D/A and A/D converters, voltage comparators, current and voltage amplifiers, Neuromorphic and artificial systems by developing chips and systems that process information collectively using predominantly analog circuits, to emulate natural signal processing, neural computational systems and biologically inspired processing systems etc.

3. LOW POWER DESIGN METHODOLOGY

As VLSI technology advances, the complexity and speed circuit increase, resulting in high power consumption. In VLSI design, small area and high performance are two conflicting constraints. The integrated circuit (IC) designer's activities have been involved in trading of these constraints. There are many possible design considerations, due to which the power efficiency has become important.

The most portable systems used in recent era, which are powered by batteries, are performing tasks requiring lots of computations. The most important aspect of Moore's Law is that it has

become a universal predictor for the growth of the entire semiconductor industry. From Moore's law, it is understood that the number of devices in a chip doubles every 18 months. This will increase the number of transistors used and hence increase the area and power consumption of the circuit.

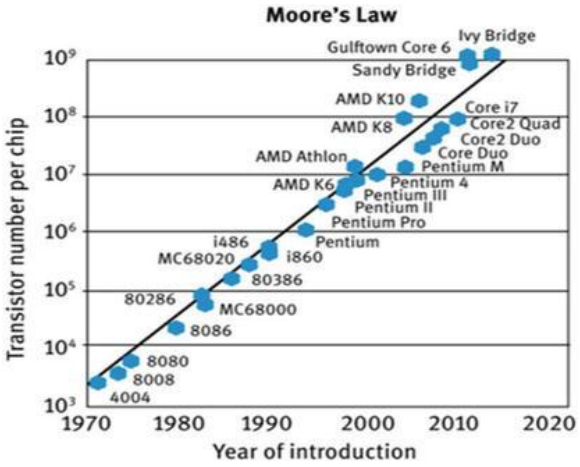

Figure 3: Graphical representation of Moore's law

4. HIGH SPEED LOW POWER DESIGN STRATEGIES WITH ANALYSIS FOR VLSI BASED MULTIPLIERS

Scaling of transistor geometries have led to integration of millions of devices in a very small space, thus driving realization of complex applications on hardware and supporting high speed applications. While the basic principles are largely the same, the design practices have changed enormously because of the increases in and transistor budgets and clock speeds, the growing challenges of power consumption, and the improvements in productivity and design tools. Device scaling has increased the operating frequency of many applications, but has led to high power consumption. This incredible growth has come from steady miniaturization of transistors and improvements in manufacturing processes. Most other fields of engineering involve tradeoffs between performance, power and price.

However, as transistor become smaller, they also become faster, dissipate less power and are cheaper to manufacture. This synergy has revolutionized not only electronics, but also industry at large. In order to reduce power, many researchers, designers and engineers have come up with many innovative techniques and have patented their ideas. Nevertheless, designers will need to budget and plan for power dissipation as a factor nearly as important as performance and perhaps

more important than area. Low power techniques have been successfully adopted and implemented in designing complex VLSI circuits.

Architecture level

As the algorithm is selected, the architecture can be determined for the given algorithm. an efficient way to reduce the dynamic power consumption is the voltage scaling. When supply voltage is reduced, the power consumption is reduced. However, this increases the gate delay. The delay of a min-size inverter (0.35 mm standard CMOS technology) increase as the supply voltage is reduced, which is shown in Fig. 4.

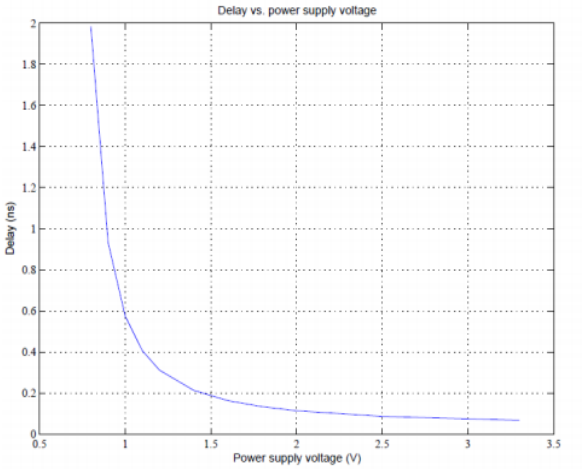

Figure 4: Graph for Delay vs. supply voltage for an inverter

To reduce the power supply voltage is used to reduce the power consumption. However, this increases the delay. To compensate the delay, we use low power techniques like parallelism and pipelining [66]. We demonstrate an example of architecture transformation.

Application in 4G communication System

4G is the next major generation of mobile cellular systems, to be deployed in near future. Tremendous consumer interest in multimedia applications requires high data rates in mobile communication system. With the advent of 4G mobile communication systems, many broadband wireless applications can be supported like video conferencing, wireless SCADA and HDTV. High capacity and variable bit rate information transmission with high bandwidth efficiency are the key requirements that the modern transceivers have to meet in order to provide a variety of

new high quality services to be delivered to the customers. 4G communication system has the following benefits as compared with 3G systems:

- Higher bit rates than 3G (20 Mbps < peak < 200 Mbps)
- Higher spectral efficiency and lower cost per bit than 3G
- Higher frequency band than 3G (below 5 GHz preferred)
- RF channel bandwidths of 20-100 MHz

Impact of power dissipation

Whenever there is power dissipation, it unvaryingly leads to an increase in chip temperature. This temperature rise affects devices when it is switched on and off. With device in OFF condition, power dissipation increases the number of intrinsic carriers n_i provided by the below relation:

$$n_j \propto e_G^{-E/T}$$

From the above equation, it is very clear that when temperature increases, intrinsic carriers also increase. With temperature increase, the less affected ones are the majority carriers which are contributed by impurity atoms. As the temperature increases further, the leakage current that depends on the concentration of the minority carrier, increases which leads to further increase in temperature.

Reduction of temperature

Heat sinks are used to dissipate heat generated by power dissipation. The thermal resistance of heat sink is lower than that of the package. So heat sink draws the heat. To eliminate heat efficiently, the rate of heat transferred to the environment should be greater than heat generated. This heat transfer rate depends on thermal resistance θ, as provided by the below relation:

$$\emptyset = 1/\vartheta_c A$$

VLSI designers have used circuit speed as the performance metric. In fact, power considerations have been the ultimate design criteria in special portable applications. The main aim of these applications was maximum battery life time, with minimum power. Low power design is also required to reduce the power in high-end systems with huge integration density and thus improve the speed of operation.

5. EFFECTIVENESS of POWER ESTIMATION TOOL

Recently, complexity levels of device size and programmable devices have grown to amazing complexity levels. Years ago, an average design had nearly twelve thousand gates. Presently, there are hundreds of thousands and sometimes multimillion gates. So when size of design increases, power consumption also increases.

Prior to the power tools, other tools have been used to provide the necessary input to the power tools. More importance is provided to the tools specifically involved in low power estimation, which has been classified as power tools and non-power tools.

Non-power tool

Non-power tools include simulation tools, synthesis tools, layout tools, extraction tools and waveform viewers.

Power tool

Varieties of power analysis tools are available to estimate the power of a design. Among them are Xilinx, Tanner, Microwind, etc. These EDA power tools are very familiar and user-friendly.

Power analysis and estimation is available throughout the design process, as shown in Figure 5.

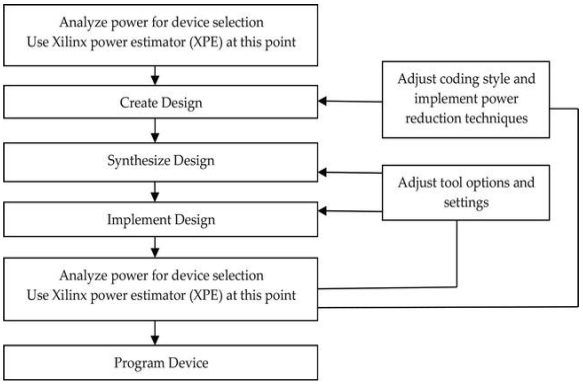

Figure 5 Power analysis flow chart

Activity rates are the basis of Xilinx Power tool. They are defined by the rate at which a logic element or net capacitance switches. Activity rates for dynamic calculations are expressed in frequency. The activity rate might be relative to clock and hence net or logic element might switch at any fraction of the clock frequency.

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Thus the main use of activity rate is in the recalculation of power and could be easily achieved by varying system clock frequency. So simulation data could be used, and this saves time. Also Xilinx Power supports several numbers of input clocks. Expressed in percentage scale, 100% activity rate means that standard signal state changes once every clock cycle. Switching rate will be the activity rate if net and logic are not clock sync.

Microwind

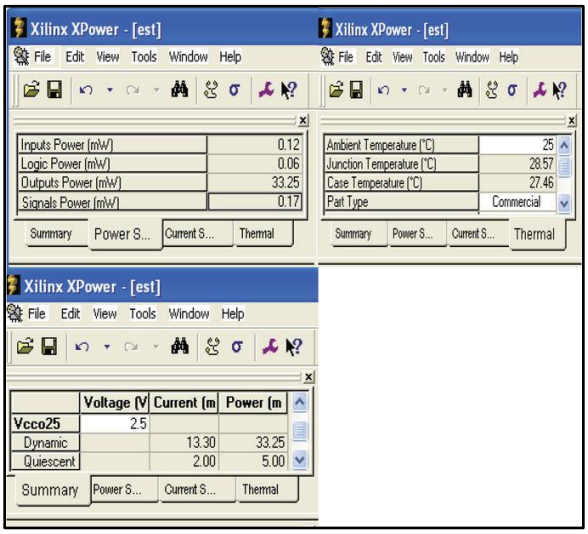

Figure 6 Power output calculation using XPower

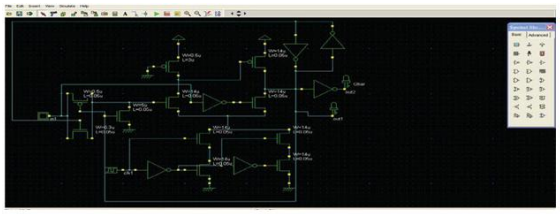

Figure 7Simulation of digital CMOS circuits

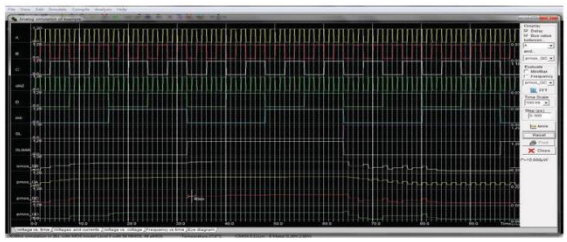

Figure 8Power calculation of digital CMOS circuits

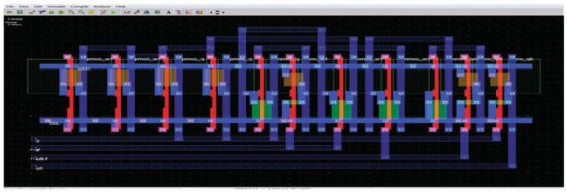

Figure 9Layout of digital CMOS circuits

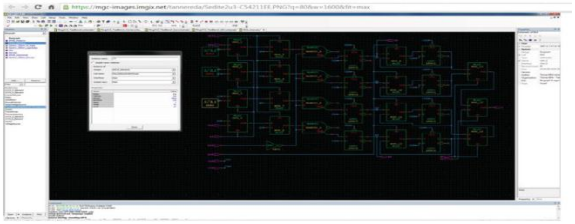

Figure 9Tanner S-Edit schematic capture

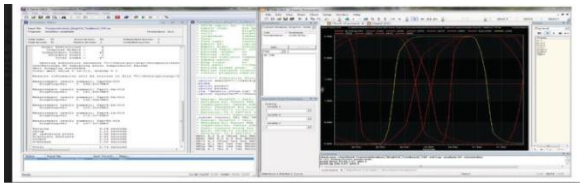

Figure 10T-spice simulation

Figure 11L-Edit IC layout

This software tool is dedicated to microelectronics and nanotechnology. The microwind software allows the designer to simulate and design an integrated circuit at physical description level. It provides innovative EDA solutions to the analog, digital and mixed-signal IC market. With MOS characteristic viewer, mix signal simulator, in-built layout editing tools, it is easier to complete design process.

Microwind unifies netlist extraction, pattern-based simulator, layout compilation, SPICE extraction of schematic, Verilog extractor, schematic entry on layout mix-signal circuit simulation, sign-off correlation, BSIM4 tutorial on MOS devices, cross-sectional and 3D viewer to deliver matchless architecture productivity and performance.

5. CONCLUSION

As the demand for faster, low cost and reliable products that operate on remote power source performing high end applications keep increasing, there is always a need for new low power design techniques for VLSI circuits. The VLSI designer's challenge is to engineer a system that meets speed requirements while consuming little power or area, operating reliably, and taking little time to design. In this work, low power techniques at circuit level, sub-system level and architecture level are addressed. 4G communication system blocks such as root raised cosine filter, digital down converter, digital up converter and digital phase locked loop is designed and implemented by adopting novel low power techniques.

With technological growth leading to demand for new products and designs with short design time and cost factors, many of the designs that have been used in designing complex VLSI circuits have not been able to adopt simple and innovative techniques to reduce power. Time to market being shorter, many engineers have not attempted or have failed to address some of the intelligent techniques that can be adopted to reduce power at circuit level, sub-system level and at the architecture level. In order to reduce power it is required to understand the architectural and functional requirements before selection of appropriate reduction techniques.

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